CLAIMS

1. A driving circuit for a plasma display panel including a plurality of cells each having a pair of display electrodes covered with a dielectric layer, the driving circuit comprising:

a scan circuit for selecting a cell to be lit; and

a sustain voltage applying circuit for applying a sustain voltage between the display electrodes of the selected cell so that sustain discharges are generated between the display electrodes for the number of times corresponding to a light intensity, the sustain voltage applying circuit including a sustain pulse generating circuit for generating a sustain pulse of a predetermined waveform and an offset pulse generating circuit for generating an offset pulse higher in peak value than the sustain pulse, the sustain pulse generating circuit and the offset pulse generating circuit being connected in parallel,

wherein the offset pulse generating circuit includes a source of a first voltage for applying a offset voltage, a first switching circuit for applying the first voltage between the display electrodes, an inductance component of generating a resonance voltage for applying the offset voltage, and a forward diode for permitting a current supplied to the display electrodes to flow forward so that the resonance voltage is maintained at a higher voltage level than a voltage level of the sustain voltage for a predetermined period of time, and

the sustain pulse generating circuit includes a source of a second voltage for applying a sustain voltage and a second switching circuit for applying the second voltage between the display electrodes.

2. The driving circuit of claim 1, wherein, when the resonance voltage level reaches a given voltage level higher than the voltage level of the sustain voltage and lower than a maximum voltage level of the resonance voltage, the first switching circuit is switched off, and after a predetermined period of time, the second switching circuit is switched on.

3. The driving circuit of claim 1, wherein the offset pulse generating circuit further includes a reverse diode and a third switching circuit, the reverse diode making a current supplied to the display electrodes to flow in a reverse direction so that a voltage level of the resonance voltage is lowered to the voltage level of the sustain voltage, the third switching circuit guiding a current to the reverse diode, the reverse diode and the third switching circuit being connected in parallel to a series circuit having the first switching circuit and the forward diode.

4. The driving circuit of claim 1, wherein the offset pulse generating circuit further includes a reverse diode, a decay inductance component and a third switching circuit, the

reverse diode making a current supplied to the display electrodes to flow in a reverse direction so that a voltage level of the resonance voltage is lowered to the voltage level of the sustain voltage, the decay inductance component lowering the voltage level of the resonance voltage by resonance, the third switching circuit guiding a current to the reverse diode and the decay inductance component, the reverse diode, the decay inductance component and the third switching circuit being connected in parallel to a series circuit having the first switching circuit, the inductance component and the forward diode.

5. The driving circuit of claim 4, further comprising a fifth switching circuit for switching on or off a short circuit which maintains a voltage applied to the display electrodes at zero, the fifth switching circuit being connected in parallel to a series circuit having the second voltage source and the second switching circuit,

wherein the offset pulse generating circuit further includes two condensers connected in series via a middle point and a series circuit for connecting the middle point and the display electrodes, the two series-connected condensers being connected in parallel to the first voltage source,

the series circuit connecting the middle point and the display electrodes including a zero level reverse diode for

lowering the voltage level of the sustain voltage to zero by making a current supplied to the display electrodes to flow in a reverse direction, a zero-level decay inductance component for lowering the voltage level of the sustain voltage by resonance, a fourth switching circuit for guiding a current to the zero-level reverse diode and the zero-level decay inductance component,

the two series-connected condensers being respectively set to have such a capacity that a voltage level of the middle point between the two series-connected condensers is almost equal to a voltage level in the middle of voltage levels of the second and first voltages.

6. The driving circuit of claim 5, wherein the first and second voltage sources are constituted of a common power source.

7. The driving circuit of claim 1, wherein the offset pulse generating circuit further includes a Zener diode for maintaining the resonance voltage at a predetermined voltage level higher than the voltage level of the sustain voltage and lower than a maximum voltage level of the resonance voltage when the resonance voltage reaches the predetermined voltage level, the Zener diode being connected to a series circuit having the first switching circuit, the inductance component and the forward diode.

8. The driving circuit of claim 1, wherein the offset pulse generating circuit further includes a third voltage source for outputting a third voltage of higher voltage level than a maximum voltage level of the resonance voltage and a third switching circuit for applying the third voltage between the display electrodes, the third voltage source and the third switching circuit being connected in parallel to a series circuit having the first voltage source, the first switching circuit, the inductance component and the forward diode,

and when the resonance voltage reaches a given voltage level higher than the voltage level of the sustain voltage and lower than the maximum voltage level of the resonance voltage, the first switching circuit is switched off while the third switching circuit is switched on, and after a predetermined period of time, the third switching circuit is switched off while the second switching circuit is switched on.